forming a gate structure of a PFET transistor above said layer of silicon germanium, said gate structure comprising a gate insulation layer, wherein said at least said portion of said layer of silicon germanium having said second concentration of germanium is positioned at an interface between said gate insulation layer and a channel region of the PFET transistor.

2. The method of claim **1**, wherein, prior to forming said layer of silicon germanium, forming a recess in said P-active region and thereafter forming said layer of silicon germanium in and above said recess.

3. The method of claim **1**, wherein said second concentration of germanium is at least 40%.

4. The method of claim **1**, wherein said second concentration of germanium ranges from 40-90%.

5. The method of claim **1**, wherein forming said layer of silicon germanium comprises performing an epitaxial deposition process to form said layer of silicon germanium, and wherein said first concentration of germanium ranges from 23-30%.

6. The method of claim **1**, wherein, after said oxidation process is performed, said second concentration of germanium is not uniformly distributed within said layer of silicon germanium.

7. The method of claim **1**, wherein performing said oxidation process comprises performing said oxidation process in a dry oxygen ambient.

8. The method of claim **7**, wherein said oxidation process is performed at a temperature that ranges from 800-1200° C.

9. The method of claim **8**, wherein said oxidation process is performed for a duration of that ranges from 30-120 minutes.

10. The method of claim **1**, wherein performing said oxidation process results in the formation of a layer of silicon dioxide on said layer of silicon germanium.

11. The method of claim **10**, wherein the formation of said layer of silicon dioxide consumes at least a portion of an original thickness of said layer of silicon germanium.

12. A method, comprising:

forming a layer of silicon germanium on a P-active region of a semiconducting substrate, said layer of silicon germanium having a first concentration of germanium;

performing an oxidation process on an exposed upper surface of said layer of silicon germanium to form a layer of silicon dioxide on said layer of silicon germanium to increase a concentration of germanium in at least a portion of said layer of silicon germanium to a second concentration that is greater than said first concentration;

removing said layer of silicon dioxide; and

forming a gate structure of a PFET transistor above said layer of silicon germanium, said gate structure comprising a gate insulation layer, wherein said at least said portion of said layer of silicon germanium having said second concentration of germanium is positioned at an interface between said gate insulation layer and a channel region of the PFET transistor.

13. The method of claim **12**, wherein performing said oxidation process comprises performing said oxidation process in a dry oxygen ambient.

14. The method of claim **12**, wherein said second concentration of germanium is at least 40%.

15. The method of claim **12**, wherein said second concentration of germanium ranges from 40-90%.

16. The method of claim **12**, wherein forming said layer of silicon germanium comprises performing an epitaxial deposition process to form said layer of silicon germanium, and wherein said first concentration of germanium ranges from 23-30%.

17. The method of claim **12**, wherein removing said layer of silicon dioxide comprises performing at least one etching process.

18. The method of claim **12**, wherein, prior to forming said layer of silicon germanium, forming a recess in said P-active region and thereafter forming said layer of silicon germanium in and above said recess.

* * * * *